BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

We claim:

1. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type disposed within the substrate;

a source diffusion region of the second conductivity type disposed in the substrate spaced-apart from the first region, a channel region being formed in the substrate between the source diffusion region and the first region;

a source electrode connected to the source diffusion region;

a drain diffusion region of the second conductivity type disposed within the first region;

a drain electrode connected to the drain diffusion region;

a buried region of the first conductivity type disposed within the first region, a first conduction channel being formed above the buried region and a second conduction channel being formed below the buried region, the buried region being spaced-apart from the drain diffusion region; and

an insulated gate formed over the channel region.

2. The HVFET according to claim 1 further comprising:

a second region of the first conductivity type disposed within the substrate, the source diffusion region being disposed within the second region.

3. The HVFET according to claim 2 further comprising

a third region of the first conductivity type disposed in the second region adjacent to the source diffusion region.

4. The HVFET according to claim 1 wherein the buried region is connected to the substrate.

5. The HVFET of claim 1 further comprising:

a tap diffusion region of the second conductivity type disposed in the first region near a perimeter boundary of the first region.

6. The HVFET according to claim 1 further comprising:

a second buried region of the first conductivity type disposed within the substrate beneath the source diffusion region.

7. The HVFET according to claim 6 wherein the second buried region extends laterally from the source diffusion region under the channel region.

8. The HVFET according to claim 1 wherein the first and second conductivity types are p-type and n-type, respectively.

9. The HVFET according to claim 1 wherein the buried region includes one or more openings that connect the first and second conduction channels.

10. The HVFET according to claim 1 wherein the source and drain electrodes include field plate members.

11. The HVFET according to claim 1 wherein the buried region comprises a plurality of buried layers that form a corresponding plurality of conduction channels.

12. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type disposed within the substrate;

a source diffusion region disposed in the substrate spaced-apart from the first region, an IGFET channel region being formed between the source diffusion region and the first region;

a drain diffusion region disposed in the first region;

a buried region of said first conductivity type disposed within the first region, the buried region forming JFET channels within the first region, one JFET channel being formed above the buried region and another JFET channel below the buried region, the buried region being spaced-apart from the drain diffusion region;

an insulated gate formed above the IGFET channel region.

13. The HVFET according to claim 12 wherein the first region has a first surface that borders a surface of the substrate.

14. The HVFET according to claim 12 further comprising:

a second buried region of the first conductivity type disposed beneath the source diffusion region.

15. The HVFET according to claim 14 wherein the second buried region extends laterally under the IGFET channel region.

16. The HVFET according to claim 12 wherein the buried region comprises a plurality of buried layers that form a corresponding plurality of JFET channels.

17. The HVFET according to claim 12, further comprising:

a second region of the first conductivity type disposed in the substrate adjacent to the source diffusion region.

18. The HVFET according to claim 12, further comprising:

a source electrode connected to the source diffusion region; and

a drain electrode connected to the drain diffusion region.

19. The HVFET according to claim 18 wherein the source and drain electrodes include field plate members.

20. The HVFET according to claim 12 further comprising:

a tap diffusion region of the second conductivity type disposed in the first region near a perimeter boundary of the first region.

21. The HVFET according to claim 12 wherein the first region is disposed in an epitaxial layer.

22. The HVFET according to claim 12 wherein the buried region includes one or more openings that connect the one and the another of the JFET channels.

23. The HVFET according to claim 12 wherein the first and second conductivity types are p-type and n-type, respectively.

24. The HVFET according to claim 12 wherein the source diffusion region has a source fingertip area, and the first region has a pair of drain fingertips

areas inter-digitated with the source fingertip area, the drain diffusion region being disposed in the pair of drain fingertip areas of the first region.

25. The HVFET according to claim 24 further comprising a buffer region disposed between the source diffusion region and the first region about the source fingertip area, the buffer region being substantially wider than the IGFET channel region.

26. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type disposed in the substrate, the first region having an above region, a below region and a lateral boundary;

at least one buried region of the first conductivity type sandwiched within the first region between the above and below regions;

a source diffusion region of the second conductivity type disposed in the substrate, an IGFET channel region being formed between the source diffusion region and the first region;

a drain diffusion region of said second conductivity type disposed in the first region spaced-apart from the at least one buried region;

an insulated gate formed over the IGFET channel region.

27. The HVFET according to claim 26 wherein the at least one buried region extends beyond the lateral boundary of the first region into the substrate.

28. The HVFET of claim 26 further comprising:

a source electrode connected to the source diffusion region; and

a drain electrode connected to the drain diffusion region.

29. The HVFET of claim 28 wherein the source and drain electrodes each include a field plate member.

30. The HVFET of claim 26 wherein the at least one buried region is spaced-apart from the lateral boundary.

31. The HVFET according to claim 26 wherein the first and second conductivity types are p-type and n-type, respectively.

32. The HVFET according to claim 26 wherein the source diffusion region has a source fingertip area and the first region has a pair of drain fingertip areas inter-digitated with the source fingertip area.

33. The HVFET according to claim 32 further comprising a buffer region disposed between the source diffusion region and the first region about the source fingertip area, the buffer region being substantially wider than the IGFET channel region.

34. The HVFET according to claim 26 wherein the at least one buried region comprises a plurality of buried layers which form a corresponding plurality of JFET conduction channels.

35. The HVFET according to claim 26 further comprising:

a tap diffusion region of the second conductivity type disposed in the first region near a perimeter boundary of the first region.

36. The HVFET according to claim 26 wherein the first region is disposed in an epitaxial layer.

37. The HVFET according to claim 26 wherein the at least one buried region includes one or more openings that connect the above and below regions.

38. The HVFET according to claim 26 wherein the at least one buried region is connected to the substrate.

39. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type;

a source diffusion region of the second conductivity type disposed in the substrate spaced-apart from the first region to form an IGFET channel region therebetween;

a drain diffusion region disposed in the first region;

a first plurality of buried layers of the first conductivity type disposed within the first region spaced-apart from the drain diffusion region, the first plurality of buried layers forming an associated plurality of JFET channels in the first region;

an insulating layer disposed over the substrate; and

a gate overlying an area of the insulating layer above the IGFET channel region.

40. The HVFET according to claim 39 further comprising:

a second plurality of buried layers of the first conductivity type disposed beneath the source diffusion region.

41. The HVFET according to claim 40 wherein the second plurality of buried layers extend under the IGFET channel region.

42. The HVFET according to claim 39 further comprising:

a second region of the first conductivity type disposed in the substrate adjacent the source diffusion region.

43. The HVFET according to claim 39 further comprising:

a source electrode connected to the source diffusion region; and

a drain electrode connected to the drain diffusion region.

44. The HVFET according to claim 43 wherein the source electrode includes a first field plate member that extends over the gate.

45. The HVFET according to claim 44 wherein the drain electrode includes a second field plate member.

46. The HVFET according to claim 39 wherein each of the first plurality of buried regions includes one or more openings that connect adjoining ones of the JFET channels.

47. The HVFET according to claim 39 further comprising:

a tap diffusion region of the second conductivity type disposed in the first region near a perimeter boundary of the first region.

48. The HVFET according to claim 39 wherein the first region comprises an epitaxial layer disposed on the substrate.

49. The HVFET according to claim 39 wherein the first region comprises a well region disposed in the substrate.

50. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a source diffusion region of a second conductivity type disposed in the substrate, the source diffusion region having a source fingertip area;

a first region of the second conductivity type disposed in the substrate spaced-apart from the source diffusion region with an IGFET channel region being formed therebetween, the first region having a pair of drain fingertips areas inter-digitated with the source fingertip area;

a drain diffusion region of the second conductivity type disposed in the first region,

a buffer area formed between the source diffusion region and the first region adjacent the source fingertip area, the buffer area being substantially wider than the IGFET channel region;

an insulated gate disposed above the IGFET channel region;

at least one buried layer of the first conductivity type disposed within the first region, the at least one buried layer forming two or more JFET channels in the first region.

51. The HVFET of claim 50 further comprising:

a drain electrode that includes a drain field plate which overlaps a portion of the first region.

52. The HVFET of claim 50 further comprising:

a source electrode that includes a source field plate which extends over the insulated gate.

53. The HVFET of claim 50 further comprising:

a tap diffusion region of the second conductivity type disposed in the first region near a perimeter boundary of the first region.

54. The HVFET according to claim 50 wherein the at least one buried layer comprises a plurality of buried layers forming an associated plurality of JFET channels in the first region.

55. The HVFET according to claim 50 further comprising:

a second plurality of buried layers of the first conductivity type disposed beneath the source diffusion region.

56. The HVFET according to claim 55 wherein the second plurality of buried layers extends beneath the IGFET channel region.

57. The HVFET according to claim 50 wherein the at least one buried layer is connected to the substrate.

58. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type;

a second region of the first conductivity type disposed in the first region;

a source diffusion region of the second conductivity type disposed in the second region, a channel region being formed between the first region and the source diffusion region;

a drain diffusion region of the second conductivity type disposed in the first region;

a buried region of the first conductivity type sandwiched within the first region to form first and second JFET channels therein, the first JFET channel being formed above the buried region and the second JFET channel being formed below the buried region, the buried region being spaced-apart from the drain diffusion region;

an insulated gate formed over the channel region.

59. The HVFET according to claim 58 further comprising:

a source electrode connected to the source diffusion region; and

a drain electrode connected to the drain diffusion region.

60. The HVFET according to claim 59 wherein the drain electrode includes a field plate member that extends over a portion of the first region between the drain diffusion region and the buried region.

61. The HVFET according to claim 58 wherein the first region comprises an epitaxial layer disposed on the substrate.

62. The HVFET according to claim 58 wherein the first region comprises a well region disposed in the substrate.

63. The HVFET according to claim 58 wherein the first conductivity type is p-type and the second conductivity type is n-type.

64. The HVFET of claim 58 further comprising:

a tap diffusion region of the second conductivity type disposed in the first region near a perimeter boundary of the first region.

65. The HVFET according to claim 58 wherein the buried region comprises a plurality of buried layers forming an associated plurality of JFET channels in the first region.

66. The HVFET according to claim 58 further comprising:

a second buried region of the first conductivity type disposed beneath the source diffusion region.

67. The HVFET according to claim 66 wherein the second buried region extends beneath the channel region.

68. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type disposed in the substrate, the first region having a laterally extended portion that forms a lateral boundary with the substrate;

a drain diffusion region of the second conductivity type disposed in the first region and separated from the lateral boundary by the laterally extended portion;

a second region of the first conductivity type disposed in the substrate;

a source diffusion region of the second conductivity type disposed in the second region, a channel region being formed between the source diffusion region and the lateral boundary;

an insulated gate disposed above the channel region;

a buried region of the first conductivity type sandwiched within the laterally extended portion of the first region to form a junction field-effect device in which current flows in the first region both above and below the buried region.

69. The HVFET according to claim 68 wherein the insulated gate extends laterally over the substrate from the source diffusion region to the lateral boundary.

70. The HVFET according to claim 68 wherein the second region is spaced-apart from the lateral boundary.

71. The HVFET according to claim 68 wherein the first region comprises an epitaxial layer.

72. The HVFET according to claim 68 wherein the buried region is connected to the substrate.

73. The HVFET according to claim 68 wherein the buried region is spaced-apart from the lateral boundary.

74. The HVFET according to claim 68 wherein the first and second conductivity types are p-type and n-type, respectively.

75. The HVFET according to claim 68 wherein the first and second conductivity types are n-type and p-type, respectively.

76. The HVFET according to claims 68, 69, 70, 71, 72, 73, 74 or 75 further comprising:

an additional diffusion region of the first conductivity type disposed in the second region adjacent the source diffusion region.

77. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type disposed in the substrate, the first region having a laterally extended portion that forms a lateral boundary with the substrate;

a drain diffusion region of the second conductivity type disposed in the first region and separated from the lateral boundary by the laterally extended portion;

a source diffusion region of the second conductivity type disposed in the substrate and spaced-apart from the lateral boundary of the first region, a channel region being formed between the source diffusion region and the lateral boundary;

an insulated gate disposed above the channel region;

a first buried layer of the first conductivity type disposed in the substrate beneath the source diffusion region;

a second buried layer of the first conductivity type sandwiched within the laterally extended portion of the first region and spaced-apart from the lateral boundary so as to act as an effective gate controlling dual current channels in the first region both above and below the second buried layer.

78. The HVFET according to claim 77 wherein the insulated gate extends laterally over the substrate from the source diffusion region to the lateral boundary.

79. The HVFET according to claim 77 wherein the insulated gate extends laterally over the substrate from the source diffusion region to the second buried layer.

80. The HVFET according to claim 77 wherein the first buried region is spaced-apart from the lateral boundary.

81. The HVFET according to claim 77 wherein the first and second conductivity types are p-type and n-type, respectively.

82. The HVFET according to claim 77 wherein the first and second conductivity types are n-type and p-type, respectively.

83. The HVFET according to claims 77, 78, 79, 80, 81, or 82 further comprising

an additional diffusion region of the first conductivity type disposed in the substrate adjacent the source diffusion region.

84. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a first region of a second conductivity type disposed in the substrate, the first region having a laterally extended portion that forms a lateral boundary with the substrate;

a drain diffusion region of the second conductivity type disposed in the first region and separated from the lateral boundary by the laterally extended portion;

a source diffusion region of the second conductivity type disposed in the substrate and spaced-apart from the lateral boundary, an IGFET channel region being formed between the source diffusion region and the lateral boundary;

an insulated gate disposed above the IGFET channel region;

a buried layer of the first conductivity type disposed in the substrate spaced-apart from the drain diffusion region, the buried layer extending through the laterally extended portion of the first region to beneath the source diffusion region, the buried layer dividing the first region into an above region and a below region, the buried layer having one or more openings which connect the above and below regions.

85. The HVFET according to claim 84 further comprising:

an additional diffusion region of the first conductivity type disposed in the substrate adjacent the source diffusion region.

86. The HVFET according to claim 84 wherein the buried layer extends beneath the drain diffusion region, at least one of the one or more openings being positioned close to the drain diffusion region.

87. The HVFET according to claim 84 wherein the one or more openings are hexagonal, square, circular, or triangular in shape.

88. The HVFET according to claim 84 wherein the one or more openings are circular in shape.

89. The HVFET according to claim 84 wherein the one or more openings are arranged in a pattern.

90. The HVFET according to claim 89 wherein the pattern is a checkerboard pattern.

91. The HVFET according to claim 89 wherein the pattern creates buried layer sections that deplete in a three-dimensional fashion.

92. The HVFET according to claim 91 wherein each of the buried layer sections are spherical.

93. A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a epitaxial layer of a second conductivity type disposed on the substrate;

a diffusion region of the first conductivity type disposed in the epitaxial layer, a junction being formed between the diffusion region and the epitaxial layer;

a drain region of the second conductivity type disposed in the epitaxial layer and separated from the junction by a portion of the epitaxial layer;

a source region of the second conductivity type disposed in the diffusion region, the source region being spaced-apart from the junction, a channel region being formed between the source region and the junction;

an insulated gate disposed above the channel region;

a buried layer of the first conductivity type disposed within the portion of the epitaxial layer spaced-apart from the drain diffusion region. the buried layer

acting as an effective gate to control dual current channels formed above and below the buried layer.

94. The HVFET according to claim 93 wherein the buried layer is spaced-apart from the junction.

95. The HVFET according to claim 93 further comprising:

an additional buried layer of the first conductivity type disposed beneath the source region.

96. The HVFET according to claim 93 wherein the insulated gate extends laterally over the substrate from the source region to the buried layer.

97. The HVFET according to claim 96 wherein the insulated gate overlaps the buried layer.

98. The HVFET according to claim 93 wherein the buried layer extends beneath the drain region.

99. The HVFET according to claim 93 wherein the buried layer is connected to the substrate.

100. The HVFET according to claim 93 wherein the first and second conductivity types are p-type and n-type, respectively.

101. The HVFET according to claim 93 further comprising:

a source electrode connected to the source region; and

a drain electrode connected to the drain region.

102. The HVFET according to claims 93, 94, 95, 96, 97, 98, 99, 100 or 101 further comprising:

an additional diffusion region of the first conductivity type disposed in the diffusion region adjacent the source region.